What is claimed is:

1. A method for forming an electronic device comprising:

forming a first conductive layer in an opening in a multilayer dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer;

subjecting the core conductive layer to a H_2 plasma treatment; and

depositing a capping adhesion/barrier layer on the core conductive layer after the H_2 plasma treatment.

2. The method of claim 1, wherein forming a first conductive layer includes depositing a seed layer on a first adhesion/barrier layer.

3. The method of claim 2, wherein depositing a seed layer on a first adhesion/barrier layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

4. The method of claim 2, wherein depositing the seed layer and the capping adhesion/barrier layer includes depositing the seed layer and the capping adhesion/barrier layer using low energy ion implantation.

5. The method of claim 4, wherein depositing the seed layer and the capping adhesion/barrier layer using low energy ion implantation includes using an implant energy ranging from about 0.1 keV to about 2 keV.

6. The method of claim 1, wherein forming a core conductive layer includes depositing the core conductive layer using a CVD process.

7. The method of claim 1, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

8. The method of claim 1, wherein depositing a capping adhesion/barrier layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

9. The method of claim 1, wherein depositing a capping adhesion/barrier layer includes depositing the capping adhesion/barrier layer having a thickness ranging from about 5 Å to about 40 Å.

10. The method of claim 1, wherein the method further includes removing at least a portion of the multilayer dielectric structure, after depositing the capping adhesion/barrier layer on the core conductive layer, to form an air bridge structure.

11. The method of claim 1, wherein forming a core conductive layer and depositing a capping adhesion/barrier layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer in the opening in a multilayer dielectric structure such that the core conductive layer and the capping adhesion/barrier layer are within one dielectric layer in the multilayer dielectric structure with a top surface of the capping adhesion/barrier layer substantially level with a top surface of the one dielectric layer.

12. The method of claim 11, wherein forming the core conductive layer and depositing the capping adhesion/barrier layer within one dielectric layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, a fluorinated oxide layer, or an aerogel layer.

13. A method for forming an integrated circuit comprising:

forming one or more device structures on a substrate;

forming a polyimide layer above a number of first level vias provided for electrical coupling to at least one of the one or more device structures;

forming a number of trenches in the polyimide layer;

forming a first conductive layer in the number of trenches;

depositing a core conductive layer on the first conductive layer;

subjecting the core conductive layer to a H_2 plasma treatment; and

depositing a capping adhesion/barrier layer on the conductive layer after the H_2 plasma treatment, wherein a top surface of the capping adhesion/barrier layer is substantially at a top surface of the polyimide layer.

14. The method of claim 13, wherein forming a first conductive layer includes depositing a seed layer on a first adhesion/barrier layer.

15. The method of claim 14, wherein depositing a seed layer on a first adhesion/barrier layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

16. The method of claim 13, wherein depositing a capping adhesion/barrier layer includes depositing material by ion implantation into the core conductive layer to form the capping adhesion/barrier layer.

17. The method of claim 13, wherein depositing a capping adhesion/barrier layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

18. The method of claim 13, wherein forming a polyimide layer above a number of first level vias includes:

forming a field oxide layer and a Si_3N_4 layer above the one or more device structures;

forming contact holes through the field oxide layer and the Si_3N_4 layer;

depositing TiN in the contact holes;

forming tungsten on the TiN to form a contact plug; and

applying the polyimide on the Si_3N_4 layer and contact plug.

19. The method of claim 13, wherein forming a number of trenches in the polyimide layer includes:

forming an oxide layer on the polyimide layer;

forming a layer of Si_3N_4 on the oxide layer;

forming a damascene image in the oxide and Si_3N_4 layers; and

removing polyimide at locations of the damascene image.

20. The method of claim 19, wherein the method further including removing the layer of Si_3N_4 using a selective etch after forming the first conductive layer, and after depositing the adhesion/barrier layer subjecting the oxide layer to an etchant that removes the oxide layer without substantially altering the polyimide layer.

21. The method of claim 13, wherein depositing a core conductive layer includes selectively depositing copper.

22. The method of claim 13, wherein depositing a core conductive layer includes selectively depositing the copper by plating in an ambient air environment.

23. The method of claim 13, wherein depositing a capping adhesion/barrier layer on the core conductive layer includes implanting zirconium ions into the core conductive layer.

24. The method of claim 13, wherein forming a polyimide layer includes forming a foamed polyimide, a fluorinated polyimide, or a foamed fluorinated polyimide.

25. The method of claim 13, wherein the method further includes a heat treatment at a temperature ranging from 250°C to about 350°C for a period ranging from about one hour to about two hours after depositing an adhesion/barrier layer on the core conductive layer.

26. The method of claim 13, wherein the method further includes removing at least a portion of the polyimide layer, after depositing the capping adhesion/barrier layer on the core conductive layer, to form an air bridge structure.

27. A method for forming an integrated circuit comprising:

forming one or more device structures on a substrate;

forming a first oxide layer above a number of first level vias for electrical coupling to at least one of the one or more device structures;

forming a number of trenches in the first oxide layer;

forming a first conductive layer in the number of trenches;

depositing a core conductive layer on the first conductive layer;

subjecting the core conductive layer to a H_2 plasma treatment; and

depositing a capping adhesion/barrier layer on the core conductive layer after the H_2 plasma treatment, wherein a top surface of the capping adhesion/barrier layer is substantially at a top surface of the first oxide layer.

28. The method of claim 27, wherein forming a first conductive layer includes depositing a seed layer on a first adhesion/barrier layer.

29. The method of claim 28, wherein depositing a seed layer on a first adhesion/barrier layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

30. The method of claim 27, wherein depositing a capping adhesion/barrier layer includes depositing material by ion implantation into the core conductive layer to form the capping adhesion/barrier layer.

31. The method of claim 27, wherein depositing a capping adhesion/barrier layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

32. The method of claim 27, wherein forming a first oxide layer above the device structures includes:

forming a field oxide layer and a Si_3N_4 layer above the one or more device structures;

forming contact holes through the field oxide layer and the Si_3N_4 layer;

depositing TiN in the contact holes;

forming tungsten on the TiN to form a contact plug; and

forming the first oxide layer on the Si_3N_4 layer and contact plug.

33. The method of claim 27, wherein forming a number of trenches in the first oxide layer includes:

forming a layer of Si_3N_4 on the first oxide layer;

applying a layer of resist;

forming a damascene image in the resist and Si_3N_4 layers; and

applying an oxide etch to define the number of trenches in the first oxide layer at locations of the damascene image.

34. The method of claim 33, wherein the method further includes after forming the first conductive layer removing the resist layer by a selective etch such that the first oxide layer is essentially unaltered by the selective etch.

35. The method of claim 27, wherein depositing a core conductive layer includes selectively depositing copper.

36. The method of claim 27, wherein depositing a core conductive layer includes selectively depositing the copper by plating in an ambient air environment.

37. The method of claim 27, wherein depositing an adhesion/barrier layer on the core conductive layer includes implanting titanium ions into the core conductive layer.

38. The method of claim 37, wherein the method further includes exposing the titanium to nitrogen to form TiN.

39. The method of claim 27, wherein the method further includes removing at least a portion of the first oxide layer, after depositing the capping adhesion/barrier layer on the core conductive layer, to form an air bridge structure.

40. A method of forming a memory device comprising:

forming an array of memory cells in a substrate; and

forming a wiring structure in the substrate coupling to the array of memory cells, at least a portion of the wiring structure formed by a method including:

forming a first conductive layer in an opening in a multilayer dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer;

subjecting the core conductive layer to a H_2 plasma treatment; and

depositing a capping adhesion/barrier layer on the core conductive layer after the H_2 plasma treatment.

41. The method of claim 40, wherein forming a first conductive layer includes depositing a seed layer on a first adhesion/barrier layer.

42. The method of claim 41, wherein depositing a seed layer on a first adhesion/barrier layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

43. The method of claim 40, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

44. The method of claim 40, wherein depositing a capping adhesion/barrier layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

45. The method of claim 40, wherein depositing a capping adhesion/barrier layer includes depositing the capping adhesion/barrier layer having a thickness ranging from about 5 Å to about 40 Å.

46. The method of claim 40, wherein forming a core conductive layer and depositing a capping adhesion/barrier layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer in the opening in a multilayer dielectric structure such that the core conductive layer and the capping adhesion/barrier layer are within one dielectric layer in the multilayer dielectric structure with a top surface of the capping adhesion/barrier layer substantially level with a top surface of the one dielectric layer.

47. The method of claim 46, wherein forming the core conductive layer and depositing the capping adhesion/barrier layer within one dielectric layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, an oxide layer, a silicon oxide layer, a fluorinated oxide layer, or an aerogel layer.

48. A method of forming an electronic system comprising:

providing a controller;

coupling the controller to one or more integrated circuits, at least the controller or one integrated circuit having a wiring structure on a substrate, at least a portion of the wiring structure formed by a method including:

forming a first conductive layer in an opening in a multilayer dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer;

subjecting the core conductive layer to a H_2 plasma treatment; and

depositing a capping adhesion/barrier layer on the core conductive layer after the H_2 plasma treatment.

49. The method of claim 48, wherein forming a first conductive layer includes depositing a seed layer on a first adhesion/barrier layer.

50. The method of claim 49, wherein depositing a seed layer on a first adhesion/barrier layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

51. The method of claim 48, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

52. The method of claim 48, wherein depositing a capping adhesion/barrier layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

53. The method of claim 48, wherein depositing a capping adhesion/barrier layer includes depositing the capping adhesion/barrier layer having a thickness ranging from about 5 Å to about 40 Å.

54. The method of claim 48, wherein forming a core conductive layer and depositing a capping adhesion/barrier layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer in the opening in a multilayer dielectric structure such that the core conductive layer and the capping adhesion/barrier layer are within one dielectric layer in the multilayer dielectric structure with a top surface of the capping adhesion/barrier layer substantially level with a top surface of the one dielectric layer.

55. The method of claim 54, wherein forming the core conductive layer and depositing the capping adhesion/barrier layer within one dielectric layer includes forming the core conductive layer and depositing the capping adhesion/barrier layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, an oxide layer, a silicon oxide layer, a fluorinated oxide layer, or an aerogel layer.

56. The method of claim 48, wherein providing a controller includes providing a processor.

57. The method of claim 48, wherein forming the electronic system includes providing a computer.

58. An electronic device comprising:

an insulating layer;

a conductive structure within the insulating layer, the conductive structure including:

a first conducting layer;

a core conductor disposed on the first conducting layer; and

a capping adhesion/barrier layer disposed on the core conductor, wherein an interface between the capping adhesion/barrier layer and the core conductor is substantially free of an oxide.

59. The electronic device of claim 58, wherein a top surface of the capping adhesion/barrier layer is substantially at a level with a top surface of the insulating layer.

60. The electronic device of claim 58, wherein the first conducting layer includes a first adhesion/barrier layer and a seed layer.

61. The electronic device of claim 60, wherein the first adhesion/barrier layer includes a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

62. The electronic device of claim 58, wherein the core conductor includes copper, silver, a copper alloy, or a silver alloy.

63. The electronic device of claim 58, wherein the capping adhesion/barrier layer includes titanium, zirconium, hafnium, or nitrides of titanium, zirconium, or hafnium.

64. The electronic device of claim 58, wherein the capping adhesion/barrier layer has a thickness ranging from about 5 Å to about 40 Å.

65. The electronic device of claim 58, wherein the insulating layer is a polymer layer, a foamed polymer layer, or a fluorinated polymer layer.

66. The electronic device of claim 58, wherein the insulating layer is a polyimide layer, a foamed polyimide layer, or a fluorinated polyimide layer.

67. The electronic device of claim 58, wherein the insulating layer is an oxide layer, a fluorinated oxide layer, a silicon dioxide layer, or an aerogel layer.

68. The electronic device of claim 58, wherein the insulating layer is disposed on a dielectric structure having a via to connect to lower level metallizations or devices in a substrate.

69. The electronic device of claim 58, wherein a portion of the insulating layer has been removed between the core conductor and another conductor to provide an air bridge structure.

70. An integrated circuit comprising:

one or more active devices in a substrate; and

a wiring structure coupled to at least one of the active devices, at least a portion of the wiring structure including:

a first level via in a first insulator layer;

a first conducting layer formed over and connecting to the first level via in the first insulator layer;

a core conductor disposed on the first conducting layer; and

a capping adhesion/barrier layer disposed on the core conductor, the capping adhesion/barrier layer, the first conducting layer, and the core conductor within a second insulator layer, wherein an interface between the capping adhesion/barrier layer and the core conductor is substantially free of an oxide.

71. The integrated circuit of claim 70, wherein the first conducting layer includes a first adhesion/barrier layer and a seed layer.

72. The integrated circuit of claim 70, wherein the first adhesion/barrier layer includes a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

73. The integrated circuit of claim 70, wherein the core conductor includes copper, silver, a copper alloy, or a silver alloy.

74. The integrated circuit of claim 70, wherein the capping adhesion/barrier layer includes titanium, zirconium, hafnium, or nitrides of titanium, zirconium, or hafnium.

75. The integrated circuit of claim 70, wherein the capping adhesion/barrier layer has a thickness ranging from about 5 Å to about 40 Å.

76. The integrated circuit of claim 70, wherein the second insulator layer is a polymer layer, a foamed polymer layer, or a fluorinated polymer layer.

77. The integrated circuit of claim 70, wherein the second insulator layer is a polyimide layer, a foamed polyimide layer, or a fluorinated polyimide layer.

78. The integrated circuit of claim 70, wherein the second insulator layer is an oxide layer, a fluorinated oxide layer, or an aerogel layer.

79. The integrated circuit of claim 70, wherein a top surface of the capping adhesion/barrier layer is substantially at a level with a top surface of the second insulator layer.

80. The integrated circuit of claim 70, further including a gap between two or more core conductors to provide an air bridge structure.

81. A memory device comprising:

an array of memory cells in a substrate; and

a wiring structure in the substrate coupling to the array of memory cells, at least a portion of the wiring structure including:

a first level via in a first insulator layer;

a first conducting layer formed over and connecting to the first level via in the first insulator layer;

a core conductor disposed on the first conducting layer; and

a capping adhesion/barrier layer disposed on the core conductor, the adhesion/barrier layer, the first conducting layer, and the core conductor within a second insulator layer, wherein an interface between the capping adhesion/barrier layer and the core conductor is substantially free of an oxide.

82. The memory device of claim 81, wherein the first conducting layer includes a first adhesion/barrier layer and a seed layer.

83. The memory device of claim 82, wherein the first adhesion/barrier layer includes a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

84. The memory device of claim 81, wherein the core conductor includes copper, silver, a copper alloy, or a silver alloy.

85. The memory device of claim 81, wherein the capping adhesion/barrier layer includes titanium, zirconium, hafnium, or nitrides of titanium, zirconium, or hafnium.

86. The memory device of claim 81, wherein the capping adhesion/barrier layer has a thickness ranging from about 5 Å to about 40 Å.

87. The memory device of claim 81, wherein the second insulator layer is a polymer layer, a foamed polymer layer, or a fluorinated polymer layer.

88. The memory device of claim 81, wherein the second insulator layer is a polyimide layer, a foamed polyimide layer, or a fluorinated polyimide layer.

89. The memory device of claim 81, wherein the second insulator layer is an oxide layer, a fluorinated oxide layer, or an aerogel layer.

90. The memory device of claim 81, wherein a top surface of the capping adhesion/barrier layer is substantially at a level with a top surface of the second insulator layer.

91. An electronic system comprising:

a controller;

one or more integrated circuits coupled to the controller, at least the controller or one integrated circuit having a wiring structure with at least a portion of the wiring structure including:

an insulating layer;

a conductive structure within the insulating layer, the conductive structure having:

a first conducting layer;

a core conductor disposed on the first conducting layer; and

a capping adhesion/barrier layer disposed on the core conductor, wherein an interface between the capping adhesion/barrier layer and the core conductor is substantially free of an oxide.

[redacted]

92. The electronic system of claim 91, wherein a top surface of the capping adhesion/barrier layer is substantially at a level with a top surface of the insulating layer.

93. The electronic system of claim 91, wherein the first conducting layer includes a first adhesion/barrier layer and a seed layer.

94. The electronic system of claim 93, wherein the first adhesion/barrier layer includes a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

95. The electronic system of claim 91, wherein the core conductor includes copper, silver, a copper alloy, or a silver alloy.

96. The electronic system of claim 91, wherein the capping adhesion/barrier layer includes titanium, zirconium, hafnium, or nitrides of titanium, zirconium, or hafnium.

97. The electronic system of claim 91, wherein the capping adhesion/barrier layer has a thickness ranging from about 5 Å to about 40 Å.

98. The electronic system of claim 91, wherein the insulating layer is a polymer layer, a foamed polymer layer, or a fluorinated polymer layer.

99. The electronic system of claim 91, wherein the insulating layer is a polyimide layer, a foamed polyimide layer, or a fluorinated polyimide layer.

100. The electronic system of claim 91, wherein the insulating layer is an oxide layer, a fluorinated oxide layer, a silicon dioxide layer, or an aerogel layer.

101. The electronic system of claim 91, wherein the insulating layer is disposed on a dielectric structure having a via to connect to lower level metallizations or devices in a substrate.

102. The electronic system of claim 91, wherein the controller includes a processor.

103. The electronic system of claim 91, wherein the electronic system includes a computer.